Comparison of Least Mean Square Based Techniques for Spur Cancellation in Fractional N-Frequency Synthesizer

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ABSTRACT

Owing to scarcity of frequency spectrum, the frequency allocation must be provided more precisely. This can be achieved by use of the systems that can maintain precise frequency control. Fractional N-frequency synthesizer is a controllable system to generate the accurately defined signals at different frequencies. In this paper, we present the LMS (Least Mean Square) based adaptive filtering methodology for spur noise reduction in digital fractional N-frequency synthesizer and investigates the noise performance response of the system against different variants of LMS algorithm. In literature only LMS was implemented, we have not only implemented different variants of LMS but also compare their performance. A digital fractional N-frequency system have been implemented in MATLAB using SIMULINK tools and noise performance of system have been analyzed in terms of SNR (Signal to Noise Ratio), spur noise and jitter by applying basic LMS, normalized LMS algorithms in adaptive filter. On comparing the performance results, normalized LMS is found to be better and efficient algorithm as it improved the system SNR by 28.09 dBc and reduces the spur noise by 9.56 dBc along with 2.9 ps improvement in jitter.

Key Words: Least Mean Square, Frequency Synthesizer, Fractional N.

1. INTRODUCTION

As frequency spectrum is limited and the allocation must be provided more precisely which can be achieved by use of the systems that can maintain precise frequency control. Frequency synthesizer is a controllable system to generate the accurately defined signals at different frequencies. A module of delta sigma modulator is used in fractional N synthesizer to generate fractional frequencies, however, it also degrades the performance of synthesizer. In the past many techniques have been proposed to achieve better performance of analogue synthesizer.

Zhang et. al. [1] presented the design of wideband fractional N-frequency synthesizer. Their proposed model uses least mean square algorithm with DAC (Digital to Analog Converter) gain calibration technique for cancellation of quantization noise and reduction of spurs by delta sigma modulator. Spur limits the performance of phase noise in wide band PLL (Phase Locked Loop) and these induced spurs cannot be reduced through loop filter. This technique requires a very precise gain mismatching of the cancellation path. Mismatching error is detected at the output of loop filter and correlated with the accumulated quantization error. Least mean square algorithm can adaptively minimize the mismatches by adjusting DAC gain according to the output errors of loop filter. Effect of DC offset at the output of loop filter can be eliminated by using differential loop filter and integrator topologies. Gain mismatch path is calibrated outside the PLL loop to avoid the non-linearity being introduced in the system [2]. When the desired reference current is achieved the gain calibrated circuit is disabled.

Analog loop filter occupies large area and its reconfiguring is difficult. To overcome these drawbacks, Elkholy et. al. [3], proposed model of digital fractional N-frequency synthesizer based on time to digital converter, digital loop filter and digital voltage control oscillator. Due to digital nature of building blocks of digital fractional N-frequency synthesizer, loop dynamics are easier to reconfigure and they are also easier to port from one process generation to other. Impact of delta sigma modulator quantization noise or error is same on digital and analogue PLL.

Simulating results of proposed work in [3] shows that at 50 MHz reference frequency PLL with bandwidth of 3 MHz generates 4.5 GHz output frequency with in band phase noise of -106 dBc/Hz and consuming 3.7 mW power. Gupta Song [4], presented the model of wideband fractional N-frequency synthesizer to achieve low phase noise by using least mean square based DAC gain calibration technique for spur cancellation. Initially DAC based spur cancellation technique is applied on first order fractional N PLLs but later on it is generalized for higher order fractional N PLLs. Spurs are generated due to non-linearity of phase frequency detector, leakage current in charge pump and harmonics generates at output of voltage control oscillator. Spur cancellation block is used to reduce the delta sigma divider ratio noise and spur correlation block is used to detect the DAC and charge pump current gain mismatching.

Digital synthesizer has all these advantages over analog synthesizer as it offers less circuitry, flexible design, low cost, and easy verification of test results. However the digital building components induces harmonics and disturbances at their respective outputs, resultantly we always get noise, spurs and jitter at the output signals of digital fractional N-frequency synthesizers [5-7]. To the best of our knowledge, no implementation of variants of LMS exists for fractional-N-frequency synthesizers. This implementation in MATLAB/SIMULINK and their comparison is our contribution.

In this paper, we implement a model of digital fractional N-frequency synthesizer in MATLAB and SIMULINK. Delta sigma modulator is the fundamental source of generating spurs in output frequency along with other blocks. As spurs usually have much higher signal powers so simple filters cannot whip it out, therefore an approach of adaptive filtering is proposed in this work where LMS [8] gain calibration technique is used to reduce the spurs.

The rest of the paper is organized as follows: Section-II will illustrate the fundamentals of analog and digital fractional N-frequency synthesizer. Section-III is based on the variants of least mean square algorithms used in adaptive filter for noise cancellation. Section-IV is composed of working, specification used in proposed model and results of model. Section-V is based on future work and conclusion drawn from simulated results.

2. NOISE CANCELLATION IN FRACTIONAL N-FREQUENCY SYNTHESIZER

Fractional N-frequency synthesizer is the most advanced form of frequency synthesizer. The function of fractional N-frequency synthesizer is to produce a periodic output signals with a frequency that is fractional ratio of the reference frequency [4].

$$F_{out} = (N + \alpha)F_{ref} \quad (1)$$

where, N is an integer. α is a fractional value between 0 and 1. F_{out} is output frequency of synthesizer. F_{ref} is input frequency.

Analogue Fractional N-frequency Synthesizer: Analog fractional N-frequency synthesizer is generally consists of PFD (Phase Frequency Detector), CP (Charge Pump), LF (Loop Filter), VCO (Voltage Controlled Oscillator), frequency divider, and $\Delta\sum$ modulator. General block diagram of fractional N-frequency synthesizer is given in Fig. 1.

Digital Fractional N-Frequency Synthesizer: Digital fractional N-frequency synthesizer is gaining more popularity due to better performance, low cost, smart in size and consuming less power as compared to the analogue fractional N-frequency synthesizer. Digital fractional N-frequency synthesizer has the same principal as of the analogue synthesizer. In digital fractional N synthesizer, time to digital converter, digital loop filter and DCO are used in place of PFD and CP, loop filter and VCO respectively.

Design of analogue fractional N-frequency synthesizer is more complex because large capacitance is required in design of analogue filter for reducing ripples in V_{ctrl}, which occupies more space. Though digital fractional N-frequency synthesizer has many advantages as compared to digital N synthesizer, but analogue synthesizer has better jitter performance. However, circuit design of digital fractional N is more flexible in terms of better test ability, programmability, and the components of digital synthesizer operate at low voltages and low in cost as well.

Adaptive Noise Cancellation Scheme: Each component of PLL introduces noise due to disturbance occurred at their outputs. Sources of noise in synthesizer are PFD, VCO, active/passive devices of DLF and quantization noise of delta sigma modulator. These noise sources affects the performance of frequency spectrum of synthesizer. For eliminating noise added by different blocks of synthesizer, adaptive filter uses the appropriate weights to estimate and remove the estimated noise signal from available information signal. Adaptive filters are widely used in applications of signal processing. These filters are usually made of FIR (Finite Impulse Response) filters for which coefficients are updated using minimization criterion. The output of adaptive filter is weighted sum of current and previous input samples. Adaptive noise cancellation scheme structure is shown in Fig. 2. The main objective of a noise cancellation system is to generate an output that is a best fit in the least square sense to the signal which can be done by applying feedback to adaptive filter then filter coefficients are adjusted using the LMS based adaptive algorithm [8].

Least Mean Square Algorithm: LMS technique was first proposed Widrow and Stearn [9]. It is the most used adaptive filter algorithm. In this algorithm, weight coefficients are adjusted from sample to sample in such a way to minimize the MSE (Mean Square Error). This algorithm is considered very reliable for noise cancellation in various communication system

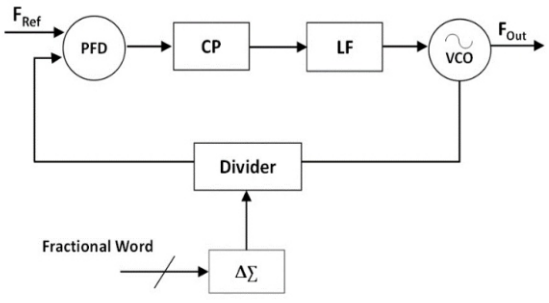

FIG. 1. FRACTIONAL N-FREQUENCY SYNTHESIZER [3]

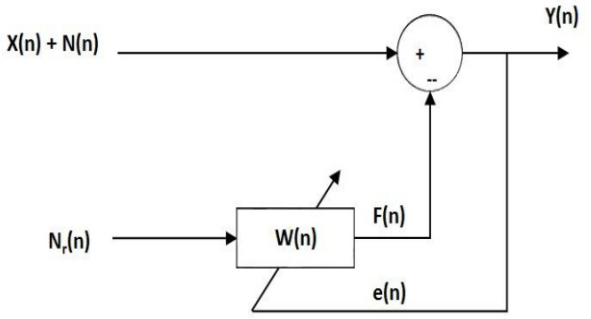

FIG. 2. ADAPTIVE NOISE CANCELLATION SCHEME [4]

applications. Aim of the algorithm is reduction of the error signal which is calculated in between output of filter and the desired signal by estimation process. The complete process is done through filtration and adaptation. In filtration, the output signal is corrupted for the adaptive filter, pertaining to the applied input signal to the filter and thus error signal is computed by taking the difference between actual output signal and desired output signal. Whereas in adaptation part, the adjustment of the filter weights is done with the help of estimated error signal [10]. The updating equation for the LMS algorithm is:

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu_e(n)\mathbf{u}(n) \quad (2)$$
$$e(n) = s(n) - y(n) \quad (3)$$

where μ is the step size of the adaptive filter, **w**(n) is the filter coefficients vector, **u**(n) is the filter input vector, d(n) is desired scalar signal and y(n) is additive noise.

Normalized Least Mean Square Algorithm: Normalized LMS is the modified form of the LMS algorithm which removes the instability problem of LMS by applying normalization to the input power. NLMS updating the coefficients of adaptive filter by using the equation mentioned in [4].

$$w(n+1) = w(n) + \mu e(n)\frac{u(n)}{\|u(n)\|^2} \quad (4)$$

Where $\mu(n) = \frac{u}{\|u(n)\|^2}$ putting this expression in Equation (4) to get the new Equation (5).

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu(n)e(n)\mathbf{u}(n) \quad (5)$$

3. SIMULATION RESULTS

To verify the impact of LMS based filtering scheme on noise performance we have implemented the model of digital fractional N-frequency synthesizer for spur reduction which deals with digital signals and uses both analogue and digital function parameters of SIMULINK/MATLAB. We have analyzed the simulation results for SNR, spur noise and jitter to assess the noise performance of our system.

Proposed Model: Digital fractional N-frequency synthesizer is a closed loop feedback system [11] that comprises of phase frequency detector subsystem, digital loop filter subsystem, voltage control oscillator, frequency divider subsystem, delta sigma modulator subsystem, LMS filter, single tone frequency estimator subsystem and jitter measurement subsystem. The working of digital fractional N-frequency synthesizer is to compare the phase of reference signal with the feedback signal i.e. divided synthesized signal through phase frequency detector and generates the phase error signal. Output of the phase frequency detector becomes the input of the digital loop filter which removes the high frequency components and allows to pass low frequency signals. The output of digital loop filter is feed to the VCO to control the oscillating frequency and phase depend upon the input signal. The output signal frequency is viewed through single tone frequency estimator subsystem and jitter is analyzed through jitter measurement subsystem. Digital output of VCO is given to frequency divider which divides down the frequency of output signal by N or N+1, this divided value is decided by delta sigma modulator. For spur noise reduction we use LMS filter. SIMULINK diagram of our proposed model is shown in Fig. 3.

Reference Signal: Reference signal of 50 MHz is generated through sine wave source block parameter in SIMULINK by using frequency in rad/sec i.e. $2\pi\times50\times10^6$ with the phase of π and sampled at $2x10^{-10}$. Sine wave block parameter generates discrete waveform which is passed through square wave subsystem to convert it in to a square wave signal.

Phase Frequency Detector Subsystem: PFD subsystem has two input ports and one output port. Reference signal and divided synthesized signal (feedback signal) are the inputs of PFD. SIMULINK diagram of PFD in time domain is shown in Fig. 4.

PFD will compare the phases of two input signals and generate the phase error. Resultantly, UP and DOWN signals are obtained at the Q output port of 1st and 2nd D flip flop respectively. Function of D flip flops is to detect the rising edge of both input signals. If the reference frequency signal is leading the synthesized signal, UP

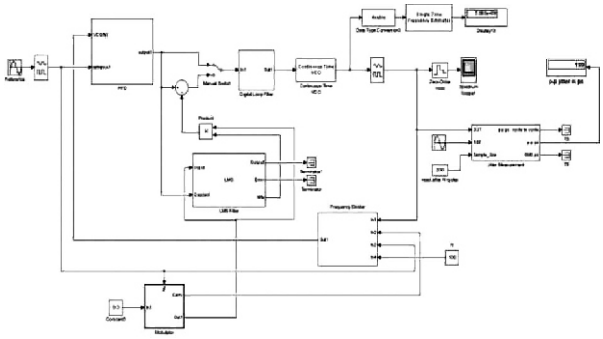

FIG. 3. SIMULINK MODEL OF DIGITAL FRACTIONAL N-FREQUENCY SYNTHESIZER

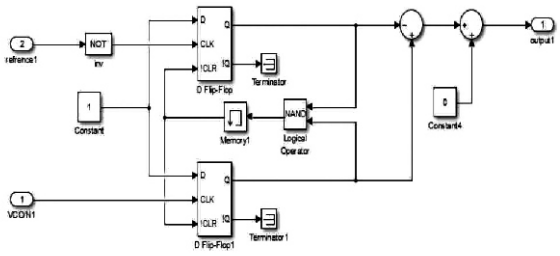

FIG. 4. SIMULINK MODEL OF PFD

signal is high and phase difference is proportional to the pulse width of Q2 therefore Q1 represents the short pulses. NAND gate is used to reset D flip flops when both Q1 and Q2 are high after a specified delay.

Digital Loop Filter Subsystem: Digital loop filter subsystem [12-13] consists of one input and one output port. Phase error generated by PFD becomes the input of digital loop filter. Digital loop filter subsystem consists of IIR low pass digital filter cascaded with proportional and integrated gains. Diagram of SIMULINK model of digital loop filter is shown in Fig. 5.

We have tweaked the parameters to allow low frequency signals to pass. We set the parameters of IIR digital filter so that it allows to pass 50-100kHz signal and set the values of proportional and integral gains i.e. 0.21 and 0.04. These gain values are used to obtain the loop bandwidth, stability and damping coefficient by using the following formulae of

Damping frequency:

$$F_n = \frac{\omega_n}{2\pi} \quad (6)$$

$$\omega_n = F_{rwf}\sqrt{K_I} \quad (7)$$

where, ω_n is natural frequency, F_{ref} is input frequency and K_I is integral gain of digital filter.

Damping coefficient:

$$\zeta = \frac{K_P}{2\sqrt{K_I}} \quad (8)$$

Where ζ is damping coefficient. K_p and K_I is proportional and integral gain of digital loop filter.

Transfer function of PI filter is:

$$H(z) = K_P + K_I \frac{z^{-1}}{1 - z^{-1}} \quad (9)$$

where K_p is proportional gain of digital loop filter and K_I is integral gain of digital loop filter.

Voltage Control Oscillator: We have used VCO function block in SIMULINK and set the parameters so that it will generate the output synthesized signal with frequency which is equal to $(N+\alpha)F_{ref}$. The output of digital loop filter becomes the input of VCO which will generate output signal of frequency range 4.797-5.163 GHz. Output frequency changes w.r.t. to the amplitude variation of the input signal. Set the parameters in VCO block parameters like quiescent frequency is 5.1 GHz and input sensitivity is 1 GHz. Spectrum of output waveform is analyzed through spectrum analyzer. Output spectrum waveform of synthesized signal frequency is shown in Fig. 6.

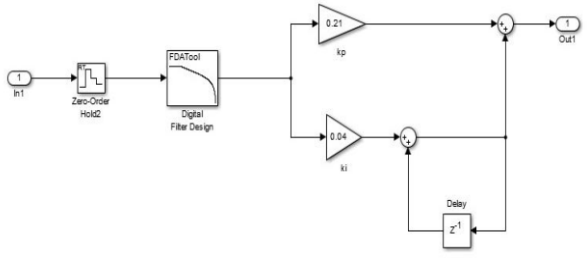

FIG. 5. SIMULINK MODEL OF DIGITAL LOOP FILTER.

Without applying LMS filter in proposed digital model, the output on spectrum analyzer in Fig. 6 clearly shows the non-uniform spread of the signal and its embedded noise which consequently results in relatively low performance in terms of SNR and jitter.

Frequency Divider: Frequency divider subsystem having four input ports and one output port. The function of frequency divider is to divided down the output synthesized frequency by the average value between N or N+1. SIMULINK model of frequency divider is shown in the Fig. 7. The output digital signal of VCO becomes the 1st input of frequency divider subsystem. 2nd input comes from carry output port of delta sigma modulator.

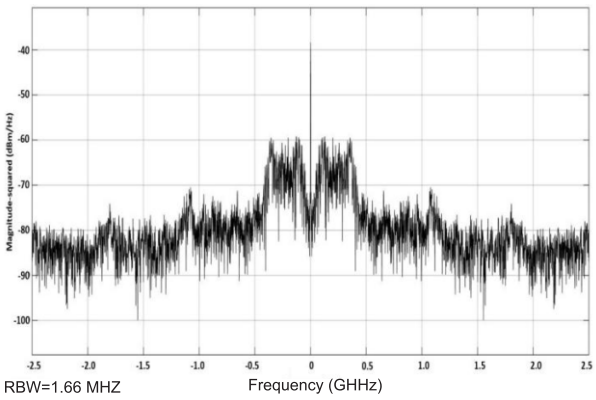

FIG. 6. OUTPUT SPECTRUM OF VCO

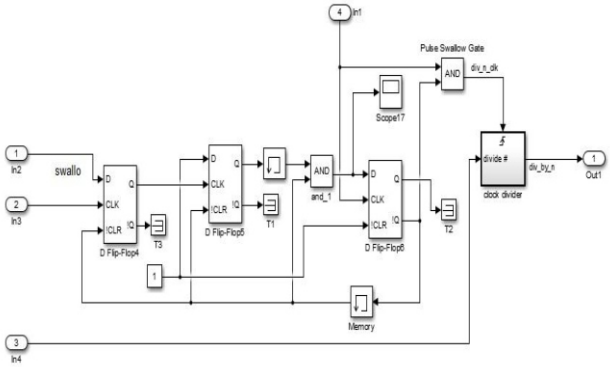

FIG. 7. SIMULINK MODEL OF FREQUENCY DIVIDER SUBSYSTEM

3rd input is the digital reference signal while 4th input is the N integer value which is used as 100 here to divide the synthesized signal frequency. The frequency divider subsystem divides the output signal frequency by N when the carry out port of delta sigma modulator is zero and divides output signal frequency by N + 1 when the carry output of delta sigma modulator subsystem is 1. α is the fractional value which is 0.3.

Delta Sigma Modulator: Delta sigma modulator subsystem having one input port and two output ports i.e. carry output port and state output port. Subsystem consists of an adder, modulator function and delay parameters. We have arranged these parameters so that carry out put port is 0 or 1 and quantization error signal is generated at the state output port. SIMULINK model of delta sigma modulator subsystem is shown in Fig. 8.

The function of this subsystem to repeatedly add the fractional value α which is 0.3 in the sum operator. When the sum is less than 1 the carry output port show 0 result. When the sum is greater than or equal to 1, carry output port shows 1 in the result. Sum operator is reset to its fractional part.

Single Tone Frequency Estimator Subsystem: Single tone frequency estimator is not the building block of digital fractional N-frequency synthesizer its function is to display the output synthesized signal frequency on display scope. We will get the different values of synthesized signal frequency with or without using LMS filter. Without using LMS filter the value of output synthesized signal frequency is 5.109GHz. The remaining values will be presented in LMS filter section.

Jitter Measurement Subsystem: Jitter measurement subsystem is also not the building block of digital fractional N-frequency synthesizer and this subsystem will help to display the jitter value on display scope. We will get different values of jitter in pico seconds with or without using LMS filter. The jitter value is 199 ps without using LMS filter.

Least Mean Square Filter: LMS Algorithm is extensively used in many application of communication due to its simplicity and robustness. The LMS algorithm can be used to minimize the mismatches between the input signals by adjusting the coefficients (gains) according to the errors at the loop filter output. We will use LMS algorithm for reduction of spur noise in proposed architecture. In SIMULINK library there is built in feature of LMS filter available. Set the parameters in LMS filter block accordingly like

Filter Length=1, Step Size (μ)=0.03 and Leakage Factor=1.

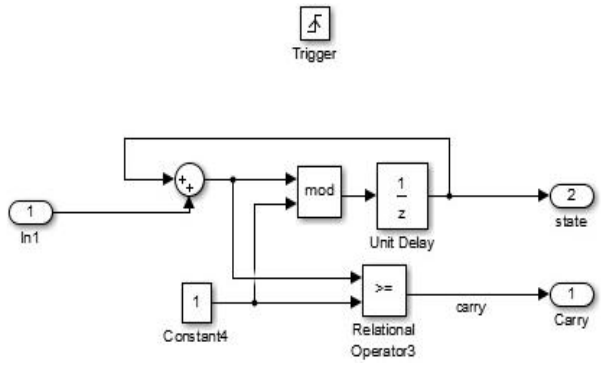

FIG. 8. SIMULINK MODEL OF DELTA SIGMA MODULATOR SUBSYSTEM

TABLE 1. RESULTS OBTAINED WITHOUT USING LMS FILTER.	
Output Frequency	5.109 GHz
Jitter	199 ps
SNR	-17.66 dBc
Spur Noise	-6.404 dBc

TABLE 2. RESULTS OBTAINED BY USING LMS FILTER.	
Output Frequency	5.138 GHz
Jitter	196.6 ps
SNR	-9.51 dBc
Spur Noise	-8.041 dBc

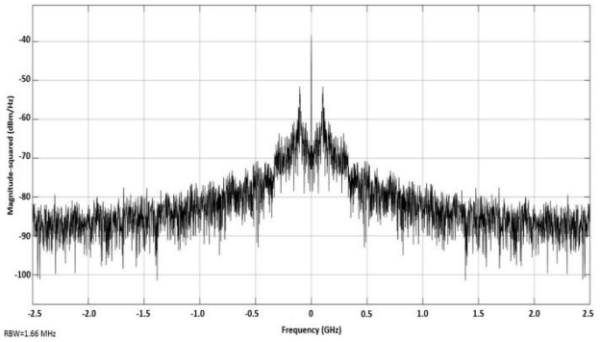

FIG. 9. OUTPUT SIGNAL SPECTRUM BY USING SIMPLE LMS FILTER

TABLE 3. RESULTS OBTAINED BY USING NORMALIZED LMS ALGORITHM IN LMS FILTER	
Output Frequency	4.797 GHz
Jitter	197.8 ps
SNR	-1.17 dBc
Spur Noise	-13.418 dBc

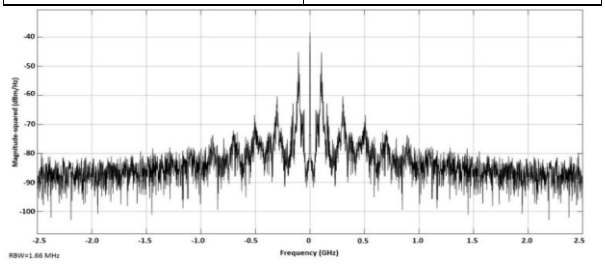

FIG. 10. OUTPUT SIGNAL SPECTRUM WITH NORMALIZED LMS FILTRE

The LMS filter offer different variants of LMS algorithm. Following are different form of LMS algorithm: simple LMS algorithm, normalized LMS algorithm, sign- error LMS algorithm, sign-data LMS algorithm, and sign-sign LMS algorithm. All the mentioned algorithms differ in the ways they adapt coefficients, regardless of how they execute convolution operations. Setting the parameters in LMS filter block and the model will shows a result in Table 2.

Fig. 9 shows the noise performance by using basic LMS algorithm based adaptive filter in our proposed digital frequency N synthesizer model, SNR is improved up to 8.15 dBc, obtain better jitter and spur noise is reduced up to 1.637 dBc.

Normalized LMS: When select the normalized LMS in LMS filter and get results mentioned in Table 3.

In Fig. 10 with the use of normalized LMS algorithm in adaptive noise filter of our model, the spectrum analyzer output is achieved with highly improved performance in terms of SNR, spur noise and jitter. Spur noise reduced up to 7.014 dBc and SNR improved upto 16.49 dBc.

Impact of Different Values of Step Size 'μ' in Noise Performance of Digital Fractional N-Frequency Synthesizer: The value of step size of LMS filter directly impacts the convergence speed, stability and steady state error of the adaptive filter. Smaller step size is used to ensure small steady state error but it also reduces the convergence speed of the filter. On the other hand, step size can be increased to speed up the convergence though it might incur instability to the filter as well. In digital fractional N-frequency synthesizer, we changed the value of step size and observed its impact on noise performance in terms of SNR, spur noise and jitter. Output values with μ=0.5, μ=1 and μ=1.2 have been summarized in Table 4 by applying simple LMS, normalized LMS, sign-error, sign-data and sign-sign LMS algorithms in filter.

It can be seen that every LMS algorithm shows different values of performance parameters on varying the value of step size (μ). However it is quite evident that normalized LMS algorithm displays the best performance as compared to any other LMS variant for each and every value of μ. It is also proven that the most optimal value of for normalized LMS is 1 where all performance parameters of digital fractional frequency synthesizer shows the best values with the improvement of SNR by 28.09 dBc, reduction of spur noise by 9.56 dBc and jitter reduction of 2.9 ps as compared to the results if no LMS filter is used.

TABLE 4. EFFECT OF STEP SIZE ON SNR AND SPUR NOISE

Output	μ = 0.03	μ = 0.5	μ = 1	μ= 1.2
Output freq	4.797 GHz	5.1 GHz	5.1 GHz	5.1 GHz
Jitter	197.8 ps	196.1 ps	196.1 ps	196.1 ps
SNR	-1.17 dBc	7.69 dBc	10.43 dBc	10.30 dBc
Spur noise	-13.418 dBc	-18.17 dBc	-15.971 dBc	-15.819 dBc

4. CONCLUSION

Though spur noise cannot be completely cancelled out however significant improvement in noise performance can be achieved by applying adaptive filters with LMS algorithm and its different versions. In our work, we have observed impact of LMS variants on noise performance of propose digital fractional N-frequency synthesizer model in terms of SNR, jitter and spur noise. Some LMS version improves one variable to some extent while the other degrades the same to different extent so there can be a tradeoff among these indicators with the use of LMS variants. If we compare the results, normalized LMS has been found to be the most efficient one to improve the system noise performance as it improves the SNR by 28.09 dBc and reduces the spurious noise by 9.56 dBc along with 2.9 ps improvement in jitter as well. We have implemented the proposed model for testing and verification MATLAB/SIMULINK as high frequency radio communication hardware chips are not readily available in Pakistan. The designing of circuit level implantation is next area of focus to evaluate the real time performance results which involves CMOS chip fabrication process as well. Apart from this, proper schematic of TDC (Time to Digital Converter) is not available in SIMULINK, so we had to use PFD in place of TDC to generate the result. Further we will try to design the TDC to simulate and study its impact on the overall noise performance of our model. Implementation of this work in hardware to validate the results is one area for future work. Another area for future research is to reduce the intrinsic noise.

5. FUTURE WORK

In future, same comparative analysis can be extended for other Adaptive algorithms like RLS (Restless legs syndrome), RMS (Root Mean Square) and APA (Affine Projection Algorithm).Analysis may be extended for comparison of more advanced performance parameters like speed, complexity and stability. Designing circuit level implantation to evaluate real time performance results. Another area for future research is to reduce the intrinsic noise.

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