A PWM-Based Technique to Measure Phase Angle Between AC Voltage and Current

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Abstract

This research paper presents a simple and cost-efficient circuit to measure the phase difference between two sinusoidal signals. We have proposed a method that converts the phase-difference into a DC voltage. A mathematical relationship between the phase difference and the DC voltage is also developed. Simulations of the proposed circuit at various phase-angles are presented, the simulation results agrees with the theoretical analysis.

Index Terms–*Power factor, Phase meter, AC load, PWM technique.*

1. INTRODUCTION

The phase difference between two sinusoidal signals can be measured by a number of methods [1-9]. M.Salamon and B. Jarc [1] have discussed the simulation results of a signal-phase meter. The authors have claimed a precise signal-phase meter with accuracy more than 0.02%. In addition, the authors have listed a few limitations of the proposed signal-phase meter including prior frequency information, and that the signal factors such; amplitude, phase, frequency, and offset voltage, should have a small rate of change and the change ought be modest. N. M. Vucijak and L. V. Saranovac [2] have proposed two algorithms named as, the simple algorithm (SAL) and a modified SAL (MSAL), for computing phase difference between two sinusoidal signals. B. Djokic and E. So have reported a nonsynchronous multirate digital filtering [3] algorithm that determines that phase angle of deformed periodic signals. The authors proposed a method that functions for a broad bandwidth while maintaining its accuracy. Earlier, S.-J. Lee et al [4] had evaluated a phase detecting technique for PWM rectifiers. While using rectifiers the voltage signal for the supply source is deformed, therefore, the true phase angle between source voltage and current becomes critical. The distortion of the source signal had been approached by applying active filters. M. A. Elela and M. Alturaigi [5] proposed a frequency-insensitive phase meter, where the phase to be measured was converted into a frequency. The frequency was measured to find the phase. R. Micheletti showed the digitizing of two sinusoidal signals and proposed an algorithm that measures the phase angle by least-square method [6].

Two interesting independent research papers, the first by S. M. Mahmud et al [7] and the second produced by K. M. Ibrahim and M. A. H. Abdul-karim [8], demonstrates the application of the dual-slop method for determining the phase angle between two periodic signals however. A classical method to measure the phase difference is to count the number of pulses in the time interval between zero-crossing of the voltage and current signal [9]. We tend to avoid this method as it has limitations of clock frequency resolution especially at low phase differences. Our proposed circuit is simple and robust and such a circuit, to the best of our knowledge, has not been presented before.

2. METHOD:WORKING OF THE PROPOSED CIRCUIT

Fig. 1 presents the proposed circuit where the main power-circuit consist of an ac voltage source, v_{in}, a current-sensing resistor R_{sen}, and an ac load comprising of load inductance L_L and load resistance R_L. As the main power-circuit input current, i_{in}, flows through the circuit, it is the phase difference between v_{in} and i_{in} that is required to measured. The remaining parts of the proposed circuit will be presented as follows.

2.1 Zero-crossing detection

One component that is used in most phase angle detection circuits is the zero-crossing detector (ZCD). The ZCD may be used as a reference or as an agent to detect the instant any electric signal crosses zero volts or amperes. The zero-crossing component in itself is a circuit and many researchers have proposed various circuit schemes and algorithms for detecting the time at which a signal experiences a zero-crossing [10]-[13]. In this research paper a conventional ZCD as presented in [13] is utilized. To detect the zero crossing of the signals, v_{in} and i_{in}, two independent ZCDs are connected. Reference to Fig. 1, the first ZCD is labeled as circuit-A and it is connected between v_{in} and ground. Circuit-A is used to detect the zero-crossing of the v_{in} signal. The second ZCD is labeled as circuit-B, it is used to detect the zero crossing of the current signal i_{in}. The voltage appearing across the input terminal of circuit-B is given as, $v_{Rsen} = i_{in} \times R_{sen}$. The resistor R_{sen} should have an insignificant value compared to the ac load. As a consequence, the voltage v_{Rsen} is trivial and has to be amplified before zero-crossing of the current i_{in} can be detected.

Fig. 2 depicts the detail schematics of circuit-A and -B, in both figures conventional ZCD as suggested in [13] has been utilized. Fig. 2(a) displays the details of circuit-A which circuit produces a pulse of short duration every time the input signal i.e., v_{in} crosses zero-volts. The output signal of circuit-A is labeled as $v_{v\text{-}zcd}$. Fig. 2(b) shows the internal circuitry of circuit-B that consists of a voltage follower, voltage amplifier, and a ZCD. The input voltage v_{Rsen} is applied to an operational amplifier based voltage follower. The voltage follower will serve to isolate the low resistance, R_{sen}, from the non-inverting amplifier and ZCD. Essentially, only the voltage across R_{sen} is transferred to the amplifier. The non-inverting amplifier is applied to amplify the trivial voltage of v_{Rsen}. Succeeding the non-inverting amplifier is a

conventional ZCD. The output of the ZCD of circuit-B is labeled as $v_{\text{i-zcd}}$.

Fig. 3 displays an exemplary timing waveforms of the proposed circuit, where the traces v_{in}, and i_{in} represent the input voltage and current signal, respectively. The time period of input voltage v_{in} is represented as T. The phase difference between v_{in}, and i_{in} is presented by θ. The traces $v_{\text{v-zcd}}$ and $v_{\text{i-zcd}}$ are the output signal of circuit-A and -B, receptively. Signals $v_{\text{v-zcd}}$ and $v_{\text{i-zcd}}$ both exhibit a pulse of amplitude V_{DD} volts every-time signals v_{in}, and i_{in} experience a zero-crossing, respectively. The remaining volts. Since $v_{\text{i-zcd}}$ is connected to the R-pin of the R-S flip flop, the short duration pulse on $v_{\text{i-zcd}}$ resets the v_{pwm} to logic zero. From time t_1 to T/2 the v_{pwm} remains at logic zero. In fig. 3, the trace v_{pwm} represents the output-Q of the R-S flip flop. It is observed that that on state (logic one) of v_{pwm} varies directly proportionally with the phase difference between v_{in} and i_{in}. From t = 0 to t_1 the amplitude of v_{pwm} is V_P volts.

2.3 PWM to DC voltage converter

The PWM to DC voltage converter stage shown in Fig. 1

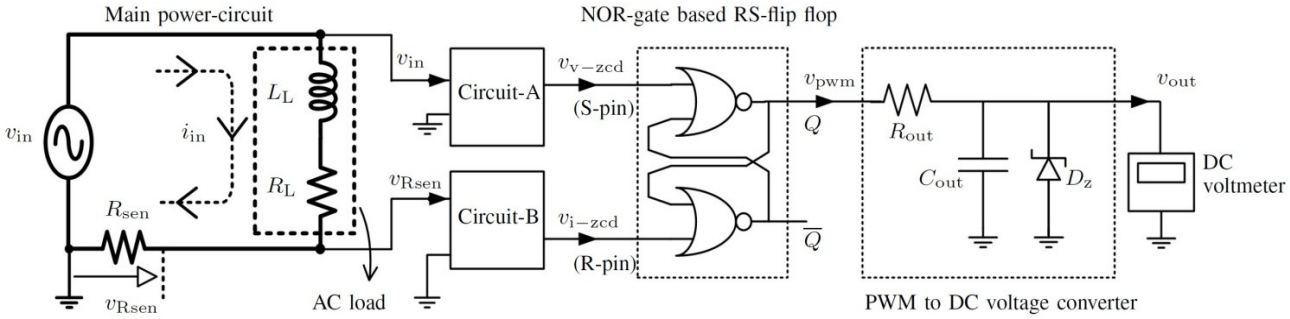

Fig. 5 The proposed circuit to measure phase difference between v_{in} and i_{in}.

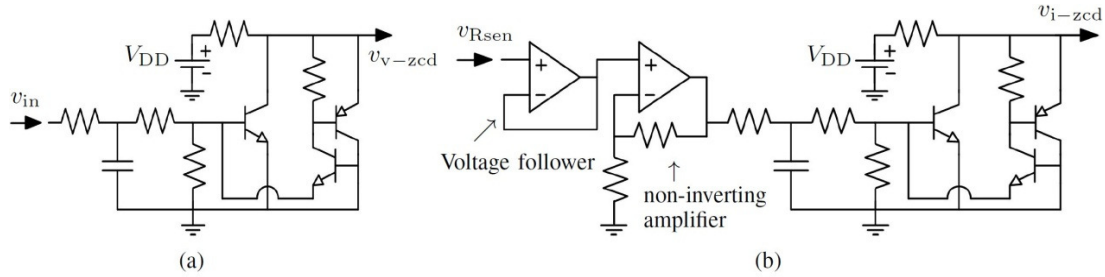

Fig. 6 Conventional ZCD circuitry [13], where (a) shows details of circuit-A, and (b) shows details of circuit-B.

traces v_{pwm}, and v_{out} will be discussed in the following sub-sections.

2.2 PWM Generation Using R-S Flip Flop

The R-S flip flop circuit shown in Fig. 1, is a sequential circuit created with the help of two NOR gates. Table I exhibits the truth-table for a R-S flip flop [14]. Briefly, the R-S flip flop output-Q with be logic one when input terminals S and R are logic one and zero, respectively. Likewise, the output-Q will be logic zero when S and R are logic zero and one, respectively. As shown in Fig. 1, the signal $v_{\text{v-zcd}}$ is connected to the set-pin (S-pin) and signal $v_{\text{i-zcd}}$ is connected to the reset-pin (R-pin), of the R-S flip flop. The output of the R-S flip flop i.e., output-Q is labeled as v_{pwm}. Reference to fig. 3, at time t = 0, the input voltage v_{in} crosses a zero volt, the signal $v_{\text{v-zcd}}$ produces a voltage pulse of V_{DD} volts for a short duration (approximately 200µs). Since $v_{\text{v-zcd}}$ is connected to the S-pin of the R-S flip flop, the short duration pulse on $v_{\text{v-zcd}}$ sets the v_{pwm} to logic one. At time t_1, the signal i_{in} crosses a zero, the signal $v_{\text{i-zcd}}$ produces a voltage pulse of V_{DD} consists of a resistor R_{out} and capacitor C_{out} circuit. The Zener diode is used for over-voltage protection. The input of the PWM to DC voltage converter stage is the signal v_{pwm}, whereas, the output of the PWM to DC voltage converter stage is v_{out}. As shown in fig. 3, the time period of the signal v_{pwm} is T/2. From circuit theory it is know that for a RC circuit, as in the PWM to DC voltage converter stage, if $5\times R_{\text{out}} \times C_{\text{out}} >> T/2$, then the voltage v_{out} appearing across the capacitor C_{out} can be expressed as,

$$v_{\text{out}} = \frac{1}{R_{\text{out}} C_{\text{out}}} \int_0^{T/2} v_{\text{pwm}} dt \tag{4}$$

With reference to fig. 3, v_{pwm} can be expressed as,

$$v_{\text{pwm}} = \begin{cases} V_P & \text{for } 0<t<t_1 \\ 0 & \text{for } t_1 < t < T/2 \end{cases} \tag{5}$$

Therefore, (1) can be rewritten as,

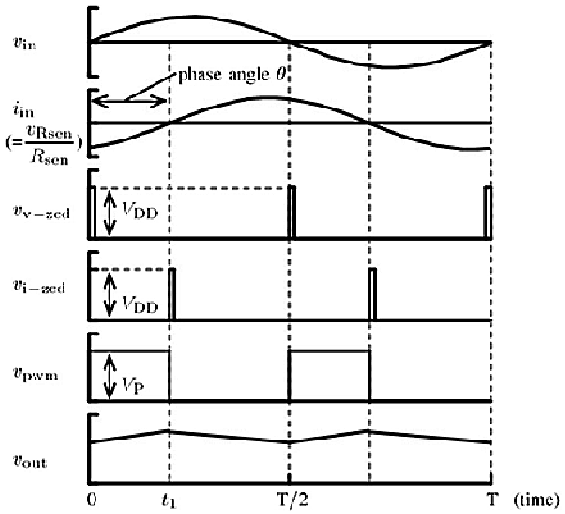

Fig. 7 The proposed circuit exemplary timing waveforms of v_{in}, i_{in}, $v_{v\text{-}zcd}$, $v_{i\text{-}zcd}$, v_{pwm}, and v_{out}.

$$v_{out} = \frac{1}{R_{out}C_{out}}\left(\int_0^{t_1} V_P dt + \int_{t_1}^{T/2} 0 dt\right) \quad (6)$$

$$= \frac{1}{R_{out}C_{out}}\int_0^{t_1} V_P dt \quad (7)$$

$$= \frac{V_P}{R_{out}C_{out}}(t_1) \quad (8)$$

Since θ =ωt, therefore,

$$t_1 = \frac{\theta}{\omega} \quad (9)$$

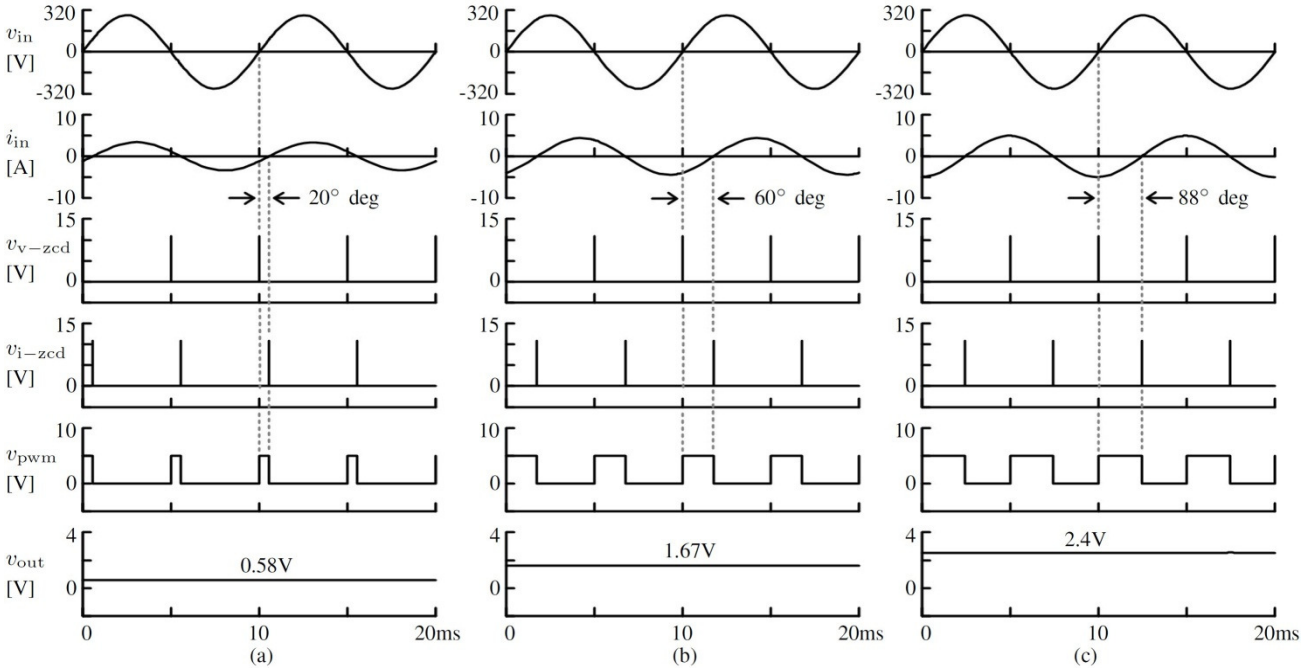

Fig. 8 Waveforms of v_{in}, i_{in}, $v_{v\text{-}zcd}$, $v_{i\text{-}zcd}$, v_{pwm}, and v_{out}. The value of v_{out} changes as the phase difference changes. (a) when phase difference is 20°deg (b) when phase difference is 60°deg (c) when phase difference is 88°deg.

Therefore, (5) can be rewritten as,

$$v_{out} = \frac{V_P\theta}{R_{out}C_{out}\omega} \quad (10)$$

That is, the phase angle θ can be expressed in terms of v_{out} can be expressed as, by rearranging (7),

$$\theta = \frac{\omega R_{out}C_{out}v_{out}}{V_P} = \frac{2\pi f R_{out}C_{out}v_{out}}{V_P} \quad (11)$$

3. SIMULATION RESULTS AND DISCUSSION

The proposed circuit presented in Fig. 1 was built and simulated in Proteus Virtual System Modeling (VSM)TM software from Labcenter Electronics™. Proteus VSM™ had been selected as it routines mixed mode SPICE circuit simulations. The circuit parameters are set as follows; V_{in} = 220V(rms), time period of V_{in} i.e., T = 20ms, R_{sen} = 1Ω, L_L = 100mH, R_L is variable from zero to 2600Ω . To apply (1), the condition 5× R_{out} ×C_{out} >> T/2, has to be maintained, therefore R_{out} is selected as 1kΩ and C_{out} as 570μF. The voltage V_P is set to 5V. The output voltage v_{out} is measured using a DC voltage meter. The phase angle is

evaluated by placing the measured value of v_{out} in (8) and solving for θ. Fig. 4 demonstrates the response of the proposed circuit for four different values of phase angle. The phase angle had been varied by varying the value of R_L. The figures presents the waveforms of v_{in}, i_{in}, $v_{v\text{-}zcd}$, $v_{i\text{-}zcd}$, v_{pwm}, and v_{out} for different values of R_L. For Fig. 4(a), R_L = 86Ω, as seen v_{out} = 0.581V, placing this value of v_{out} in (8) reveals θ = 20°deg. At the same time, the phase angle can be calculated from the formula,

$$\theta_{calc} = \tan^{-1}\left(\frac{\omega L_L}{R_L}\right) \quad (12)$$

Placing L_L=100mH and R_L=85Ω in (9) gives θ_{calc} =20.2°deg. Similarly, keeping L_L same as before and changing R_L to 18Ω, the

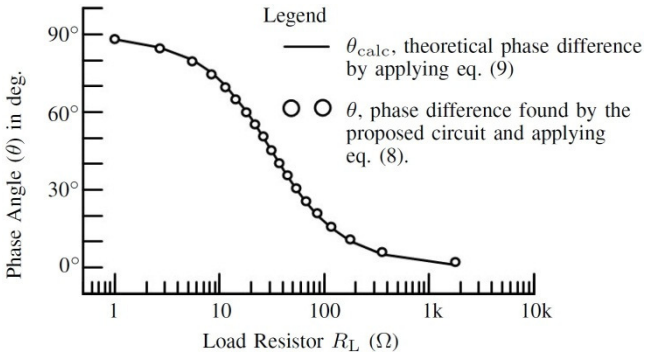

Fig. 9 Comparison of the phase-difference obtained theoretically i.e., θ_{calc} verses θ, found with the help proposed circuit.

DC voltage of v_{out}=1.67V and the evaluated phase angle θ from (8) 59.8°deg, whereas the calculated phase angle θ_{calc} =60°deg. Again reference to fig. 1, if R_L=1Ω then the v_{out}=2.46V and phase angle θ=88°deg, whereas the calculated phase angle θ_{calc} =88.1°deg.

To further test the proposed circuit, the load resistor R_L was varied from zero to 2600Ω whereas the load inductance was kept constant of 100mH and the capacitor C_{out} voltage i.e., v_{out} was observed. The phase angle θ was found from the value of v_{out} and compared with the phase angle θ_{calc}. Fig. 5 present the comparison, the agreement between θ and θ_{calc} substantiate the proposed circuit. However, the observed difference between θ and θ_{calc} is due to the insertion of current sensing resistor R_{sen}. For example when R_L had been set to zero-ohms the total resistance of the circuit was 1 due the R_{sen}.

4. CONCLUSION

The objective of this paper was to present a model of a PWM based measurement of phase angle. The proposed circuit was simulated and results were compared with the theoretical results. The simulated results agreed with theoretical results. The proposed model is simple to build and low-cost. Since the proposed circuit produces a DC voltage that is proportional to the phase angle, this DC voltage can be easily converter to a digital signal for applications to microcontrollers, personal computers, or DSP cards.

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